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Design of CMOS GHz Cellular Oscillator/Distributor Network with Supply Voltage and Ambient Temperature Insensitivities

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Abstract. GHz level ultra high speed clock generation and distribution for synchronization becomes a very important technical issue in chip and SoC applications. This paper proposes a novel way of CMOS GHz cellular oscillator/distributor networks with inherent insensitivities to supply-voltage and temperature fluctuations. Simulation results prove that maximun clock skew is limited within ~1% of a system clock period, given 3% of power supply and/or 5% of temperature fluctuations. This technique can thus be used for a low skew clock distribution in a few GHz speed VLSI and SoC systems design. The SPICE simulations are carried out with 3V, 0.5μm CMOS N-well process parameters to prove the novelity as well as the validity of the idea. Layout is also included for the future chip fabrication.

Keywords:. CMOS GHz Oscillator, Clock Generation and Distributtion, Synchronization, Performance Degradation, Supply Voltage/Ambient Temperature Insensitive Circuit, Clock Skew, Jitter.

1 Introduction

The most popular and currently widely-used solution for a ultra-high-speed synchronization is Phase Locked-Loop (PLL) [1]. Along with symmetric clock line layout schemes, the PLL is known to provide within a few pico-second degree of clock skew, or jitters. However, the physical nature of the clock line material characteristics, the jitters are still a limiting factor of systems overall performance, causing synchronization malfunctions [6, 8].

In this paper, a novel way of GHz clock generation and distribution technique is newly proposed. This technique, called Cellular Oscillator Network, adopts a fractal structure of a very simple oscillator, which can spread both in 2D and also in 3D space in the digital systems. Due to the inherent fractal structure, it minimizes the jitters caused by local gradients, yielding global averaging and thus minimized disturbances for each and every clock nodes instantly.

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2 Cellular Oscillator and Distributor Networks Circuit

2.1 Structure of Cellular Oscillator Networks

Fig. 1 shows the structure of the Cellular Oscillator Network (CON). As seen, the CON has a fractal modular structure, theoretically spreadable infinitely. Each branch performs an inverting function.

Each node can be implemented with an inverter, as the simplest form, or any logical inverting circuitry, and each loop consists of odd number of inverting nodes, which acts like a type of ring oscillator. In this scheme in Fig. 1, each node generates three different oscillating signals, with $2/3\pi$ phase shift among them [4, 6]. And signals will theoretically have exact 50% of duty cycle.

Notice here even with a frequency change or a phase shift in one or several nodes in the networks, this local disturbance will spread out to the entire networks, yielding an instant (depending on the speed of the node) global state change [4].

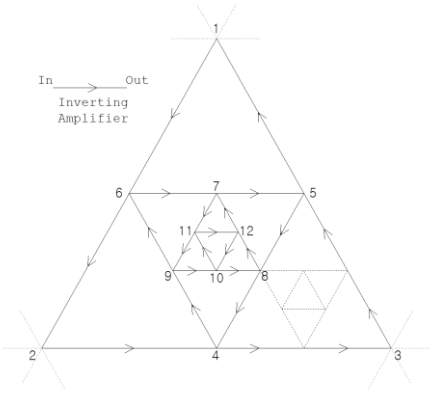

Fig. 1. Fractal structure of Cellular Oscillator Network.

2.2 CMOS Oscillator Network with an inverter for each node

Fig. 2 shows an example of CMOS cellular oscillator network that is made of 108 inverters. The way how to implement the CON is displayed in Fig. 3. Notice in this scheme shown in Fig. 1, there will be an instant global clock signal distribution with unbalance load conditions, and in this paper, even with local power supply and/or temperature disturbances.

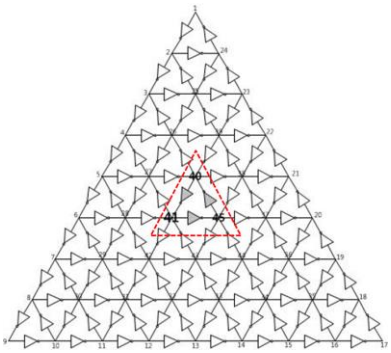

Fig. 2. CMOS Cellular Oscillator Network with 108 inverters.

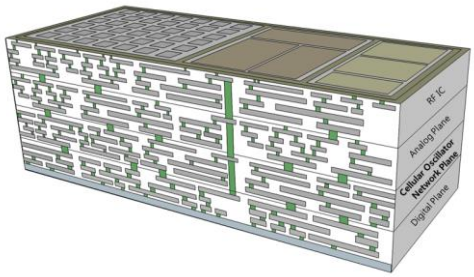

Fig. 3. The CON silicon implementation in multilayer CMOS/ multi-chip module package technique.

2.3 Clock skew simulation of Cellular Oscillator Network

Simulation results in time domain of the Fig. 2 is shown in Fig. 4. As seen in figure above, 15 nodes generate exact same signals. And the rest two sets of in-phase clock signals are also measured the same with only 120 degree of phase shifts.

3 Simulation results with power supply voltage/temperature change and CMOS layout

Simulations were done with CMOS n-well technology, along with 3V, 0.5um minimum feather size (both N- and P- MOS) condition. Supply voltage is assumed changing 3% range, while the temperature is fluctuating within 5% of a given ambient temperature, -40℃ ~ 85℃.

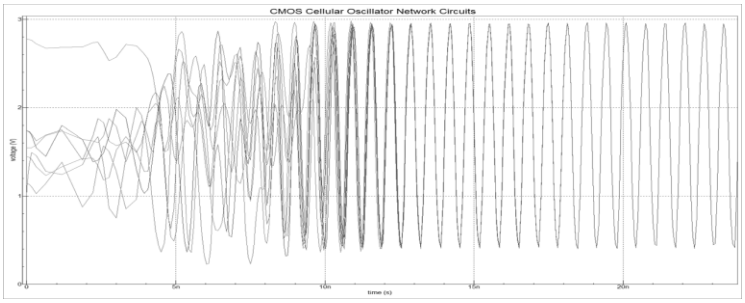

Fig. 4. Fifteen in-phase nodes simulation results.

3.1 Clock skew simulation with supply voltage variations

Fig. 5 shows clock skew simulation measurements when power supply is changing locally up to 2, 5, and 8%, respectively. The (a) is when the local change is given only in the internal loop (node 40, 41, 45) and the (b) is for the outer loop (node 16, 17, 18).

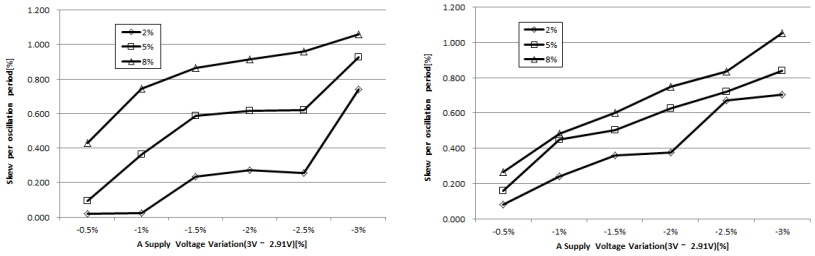

Fig. 5. Clock skews with local power supply voltage change: (a) inner loop and (b) outer loop

Table 1. Skew variation results for a local supply voltage change (Center and Corner).

The Center of Networks at Supply Voltage Variation								
Volt Variation			-0.5%	-1%	-1.5%	-2%	-2.5%	-3%
Skew Rate[%]	Cell Area	2%	0.021	0.023	0.235	0.273	0.257	0.742
		5%	0.095	0.364	0.587	0.618	0.620	0.929
		8%	0.430	0.745	0.866	0.916	0.960	1.061
Supply Voltage Range : 3 ~ 2.91V								
The Corner of Networks at Supply Voltage Variation								
Volt Variation			-0.5%	-1%	-1.5%	-2%	-2.5%	-3%
Skew Rate[%]	Cell Area	2%	0.081	0.240	0.361	0.375	0.672	0.703
		5%	0.159	0.451	0.502	0.628	0.722	0.841
		8%	0.265	0.483	0.602	0.748	0.836	1.054

As read from the Table 1, maximum of ~1% of clock period is measured among in-phase nodes with 8% of supply voltage is given. The insensitivities for a local supply voltage fluctuation is clearly witnessed.

3.2 Temperature

Local temperature change is given, from 0% up to 100% for the whole nodes, and the skew was measured for each case. Fig. 6 shows the simulation results.

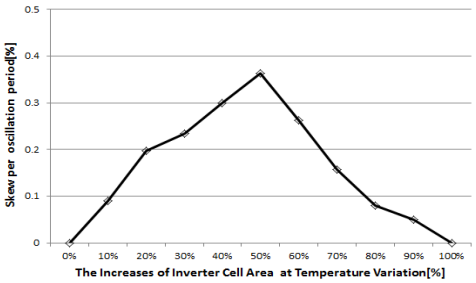

Fig. 6. Clock skew variation with a different local node numbers (%).

As seen, the more nodes (cells) have temperature changes, the more skew is measured, at 50% the largest of 0.35%.

Table. 2. Skew variations for maximum 5% of temperature change.

Temp Variation	-5%	-3%	-1%	0%	1%	3%	5%
Skew Rate[%]	0.347	0.095	0.062	0	0.065	0.185	0.340
Operation Temperature Range : -40 ~ 85℃							

As read from the Table 2, the clock skew by temperature change of 5%, a less than 0.4% skew of a clock period is measured. And this seems quite robust to the local temperature change over the system clock distribution performance.

3.3 Layout

Fig. 7 is a CMOS layout of 108 interver CON shown in fig. 2.

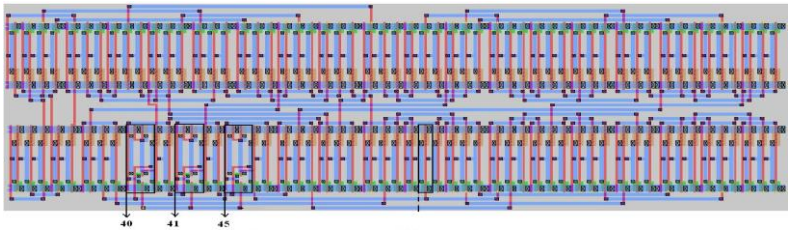

Fig. 7. CMOS layout of Fig. 2.

4 Conclusions

A new way of ultra-high speed clock generation and distribution technique is proposed and designed for its robustness proof with power supply voltage and temperature changes. With its inherent fractal structure, the cellular oscillator network is proven to have less than 1% and 0.4% clock skews of a clock period with given 3% of power supply and 5% of temperature fluctuations, respectively. This implies that the CON can be adopted in GHz clock generation and distribution in a single chip, and chip-to-chip and system-to-system (SOC) applications as well. The proposed CON is being implemented in CMOS design, and under chip fabrication for a test.

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