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Study on bus assignment algorithm for SOC test

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Abstract. The main concern is over rising temperature during the testing of complex system-on-chip (SOC), this paper studies SOC wrapper and test access mechanism (TAM), and proposes an improved algorithm of TAM assignment under the constraints of temperature. The algorithm uses temperature superposition method and adds compression process. This algorithm can find the test structure that uses shorter test time.

Keywords: TAM, thermal constraint, temperature superposition method, compression process.

1 Introduction

Many challenges are proposed in chip design, test and validate along with the enhancing of SOC integration and complexity. First of all, because the IP core is generally buried deep inside the chip, it can not be accessed, tested directly. This requires a properly designed test structure for accessing the internal IP. Secondly, due to the power dissipation rises and temperature sharp rise during the test, the temperature is taking into account when test structures are designed. The design must be constrained by temperature.

General test case is designed conform to the IEEE 1500 standards. IEEE 1500 standard provides a series circuit as IP core test case basic structure. It has four main components: interface pins, including the serial input/output WSI-WSO, parallel input/output WPI-WPO, control interfaces such as WIP, control orders generally offered by WSI and WSO transmission ,test data can be transmitted over the WPI-WPO, can also be transmitted through the WSI-WSO serial ; Shell instruction register WIR are used to control the test case work mode; WBY the bypass register are used to bypass other data registers, providing a fast data transmission channel; the testing boundary unit WBR are used to input stimulus and output response to achieve controllability and absorbability of IP core [1]. Test case design's main job was to divide the shell scan chains, which correspond to different TAM width, find the shortest test vectors transfer time.

In order to conduct parallel testing, test bus is usually to be grouped. The IP core in different groups can be tested at the same time. It either is grouped by fixed-width or as a grouping variable. In the fixed-width testing bus structures, private bus is divided into more than one group, each group the bus width is same, and can be tested

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simultaneously, enabling parallel testing. When the same group of IP core for testing, other IP core test case to bypass them, without prejudice to the current IP-core test. This structure although can achieved parallel test, but due to different optimal test width of each IP core, so bus utilization is lower; in the test bus width variable structure, bus distribution is according to optimal of principles, each group bus is distributed to different IP core different bus width, that grouping is more flexible, and test bus can be used more efficient [2].

2 Test case and test access mechanism for joint design algorithm

Generally when the test case and test access mechanism for system-on-chip is designed according to the chip's design requirements, special test bus width is given, as well as IP core parameters, such as the number of inputs, outputs, and test vectors, and the internal scan chain number and length. Test structure design's goal is to complete each IP core wrapper design, identify the assigned TAM bus and determine the order of each IP core test, make the whole testing process of the shortest time, and restrict the test power and temperature in a specified range.

Designing algorithms can be divided into two main parts, the first part is the wrapper design algorithms, correspond to different TAM width designs test cases for each IP core in a different TAM bus width; the second part is the TAM bus assigned algorithm, according to the data obtained in the first part, bus are distributed and the IP core test orders is identified, the test design is completed. This paper mainly introduces the second part.

3 TAM bus allocation algorithm

TAM bus allocation algorithm can effectively allocate bus to each IP cores, maximize bus utilization. The total time of the test is reduced by parallel testing. Thomas Edison proposed TAM bus distribution algorithm under temperature limit [3]: IP core test process can be represented by use of rectangle block, the width of rectangle block said test occupy of TAM width, and the length said test of time, each test process corresponds to a rectangle block. The problem of bus distribution can equivalent for II dimension boxing problem: given width of box for limited value, length for unlimited value. It requires all rectangular block to be assembled into the box, and temperature constraint must be satisfied during the packing process, so it takes up the Minimum length of the box. Figure1 shows the algorithms assigned TAM bus example.

This paper improved Thomas Edison Yu packing algorithm. It replaced temperature transport model with temperature superposition model, and added the compression process in the allocation of test bus under temperature constraint. The algorithm is divided into four parts, beginning with defining TAM preferred widths.

According to the wrapper design algorithms, we know that, when TAM width smaller, test time is a sharp drop along with the increase of TAM width, and when the width is increased, the decline was significantly reduced, as shown in Figure 2. In order to do not take up too much of bus resources and make the IP core cannot be

tested in parallel, the algorithm do not use the widest Pareto - optimal point as the preferred width. It used constant P compromise choice test time TP (i), then found the closest width W between TP (i) and the test time, and set the width to its preferred width.

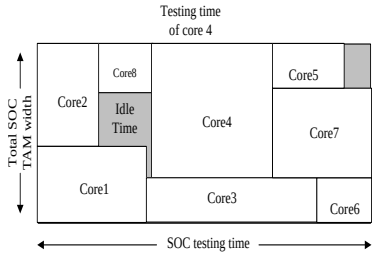


Fig. 1. boxing problem

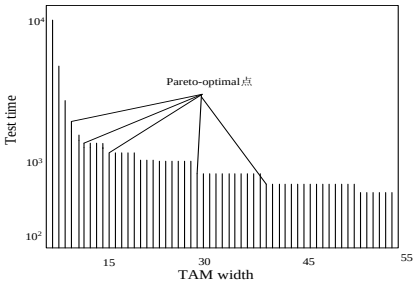


Fig. 2. TAM width and test time relationship

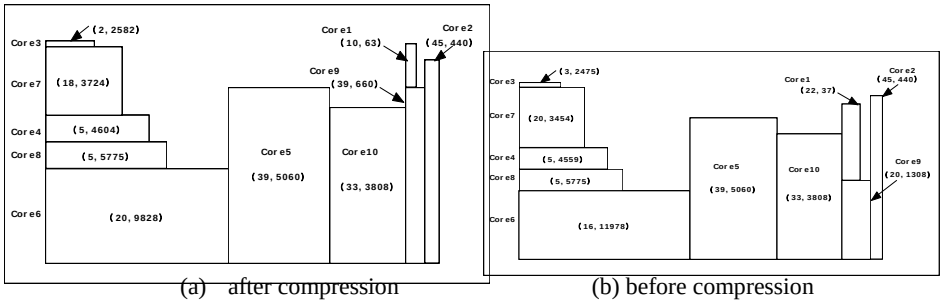
P value is usually between 1 to 10.When the difference between the IP core widest Pareto-optimal points and preferred width is less than d, set preferred width to widest Pareto-optimal point, which effectively reduces the overall testing time, especially when the IP-core test time is greater than the maximum test time for all IP core, the effect is particularly evident. The literature [4] gives a detailed description of example for the method of selecting the preferred width.

Secondly, TAM bus was assigned. The program is subject to while loops until the IP core are allocated, the loop body contains three kinds of distribution, and the first allocation methods is: In the present moment, the IP core that is not yet to be tested is found, its preferred width will be less than the current width available, and its testing time will be the longest time. The preferred width is distributed to that IP core. The second kind of allocation methods is: when the first allocation could not be found to meet the requirements of IP core, the second approach is performed. The IP core that its preferred width is less than or equal to the current available TAM width plus three is found. And the widest Pareto-optimal points that meet the requirements are assigned to the IP cores. Constant three is the data of a large number of experiments result, can be modified appropriately according to actual condition, in order to achieve a better distribution effect. The third allocation is: when the IP core cannot be found to meet the requirements with above two methods and TAM width currently available was not all allocated, you can widen the assigned bus in order to reduce bus idle time, and find the IP cores that start a test at this moment, put the rest of the bus allocated to it.

Temperature superposition model considers the temperature of several IP core to be tested at the same time equal to the temperature sum of each IP core to be tested separately [5]. In order to reduce idle time during testing, this paper reduces idle time through the compression process, thereby shorten test time. In figure 2, by broadening bus width of core1, core8, and reducing the test bus width of core2, idle time behind Core2 can be compressed. This improvement process is known as compression process.

4 Conclusions

We perform the following experiment to illustrate the effectiveness of the compression process to reduce the test time: Set the maximum width of 50, the highest temperature of 98.2 ℃, Design result of d695 in ITC 02 standard circuit is shown in figure 3.The figure (a) shoes the case by use of the compression process, and the figure (b) is the case before compression process. The testing time is 19796 in figure (a) and 22594 in figure (b) educes 2798 after compression process. The total testing time reduced by 12.4%.



(a) after compression (b) before compression

Fig. 3. The effect of compression

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