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Implementation of Instrument for Testing Performance of Network Crossing Sub-network

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Abstract. In connection with testing the performance of crossing sub-network ，this paper provided the design idea of the instrument based on LINUX system platform for testing network performance，and the detail test schedule ． The paper discussed the key technique which concerns construction and parse of the test frame based on hardware，the software design flow in testing process as well． The test data reflect the performance of bidirectional throughout of the tested router． The test results indicate that the design idea and test schedule are viable，which is effective for testing performance of network．

Keywords: test across subnet; 2544 test; throughput; Qt; loopback test frame

1 Introduction

The performance of Internet will directly influence the network size, network stability and reliability. It is necessary to have real-time performance test to evaluation and analysis of the quality Ethernet Service (QoS) So the Instrument for Testing Performance of Network is necessary to evaluate the performance of various types of network and network acceptance

This paper introduces a new type Instrument for Testing Performance of Network .it use Linux as a system software platform, and S3C2440 is used as the core processor. And using large-scale FPGA circuit to realize network。 Meanwhile the Testing Performance of Network Crossing Sub-network is innovatively proposed and realized

2 RFC2544 testing standards

One of the important test indicators of Network performance testing is described in RFC2544 .The specific test methods about network performance testing is described in RFC2544 . Four key indicators is defined in RFC2544 mainly: throughput, latency,

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Lost Rate, and Back-to-Back. These indicators are the basis for the evaluation of network equipment, and the basis for the evaluation of Ethernet devices and networks, suitable for all Ethernet connectivity devices and network 。 In the test, setting up the test conditions are very important, such as test packet length, test time, test speed and so on. Tested under diverse conditions, there will be different in the test results.

Conduct RFC2544 tests include two kinds of methods. Test configuration includes two kinds, one is the purpose of dual-port tester for testing, because it is on the same test instrument, so I do not clock synchronization problem. However, due to the dual-port design, reducing the amount of the test apparatus, there is a defect site application inconvenient. In the design, taking into account the actual instrument applications and application objects, using another method that uses two sets of test equipment, including a test as a master, a variety of tests, the other one as a data loop back side implementation data on network performance loopback test frames. For this kind of test case, test parameters, test results are bidirectional.

3 Hardware Design

The network test instrument includes the data acquisition module hardware system and data processing and analysis module software system based on RFC2544 test design and development.

The hardware module is responsible for data acquisition using the high performance FPGA circuit to realize, on the basis of FPGA circuit we run embedded Linux system to complete the entire data transceiver control function, accept the upper software commands and data interaction function; FPGA chip is mainly to complete the line speed data generating and receiving, timing processing and counting statistics and other functions.

The software module take data processing and analysis, using simple and flexible man-machine dialogue interface, supporting for TCP/IP protocol.

During the network performance testing of the different subnets, two test instruments are usually accessed to different subnet segment, one tester is used as the host sending data of the test frame, the other one is set to loopback . In the design of the test, the network address settings and connection diagram is shown in figuer1. In the testing process, we need to set the tester routing on the router to make sure that the UDP test frame can reach the test instrument in the subnet.

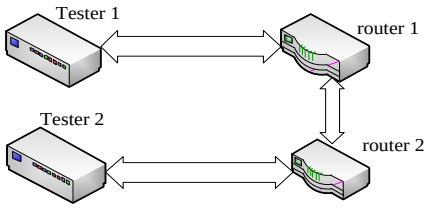

Fig. 1. test router connection

In the design, during the throughput test, we adjust the send rate with bisearch algorithm till the send frame of the DUT equal to the received frame of the DUT, the wire-speed stepping rate is 1%. Owing to the instrument need to strict control byte time parameters, using software methods cannot meet the needs of the actual test due to the long time delay, low precision. Therefore, using the method of the hardware timer is necessary, so the time precision can be achieved one byte, namely 12.5 NS. The sender adjusts the wire speed by adjusting the test frame interval and the data flow interval..

The test frame circuit is mainly in the FPGA, including sending RAM, address generator, CRC checksum, framing and other circuits. The encapsulating timing circuit manage to read out a variety of software data ,which is edited by the sofwware and stored in the RAM . According the real time, The encapsulating timing circuit also inserts the precise time identifier corresponding number of the test frame, which make it easy to test the network delay or other parameters.

Deframing circuit gets UDP testing frame data and the relevant test frame time parameters of the MAC frame. In order to calculate the network time parameter and the network packet loss rate.,

4 The software design

The embedded Linux operating system has the kernel small, good stability, strong versatility, no copyright trial fee and many other advantages, so it is the preferred.The software design adopts the hierarchical design, the design hierarchy diagram as shown in figure4.

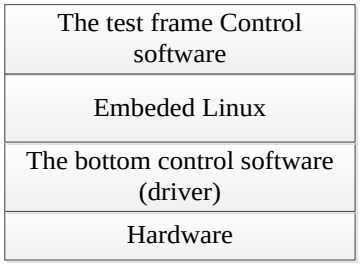

Fig. 4. the whole software hierarchy diagram

The device driver is an important part of the Linux kernel. It is interfaced between the operating system kernel and the machine hardware, the main work is to complete a read operation on the statistics register in the design, including the test frames send counter, test frame reception counter. And take the operation of the receiving RAM data area, interrupt mode to loop back

data and related statistical register operation. Design for all of the equipment are designed as a character device.

The system uses Qt- Embedded-4.5 for the development of human-machine interface. Complete the design of the main interface and the sub interface in Qt Designer, and uses Qt to realize the interface switch as well as the man-machine interface and the underlying SCM control system interaction.

In the application layer software design, we realize data loopback frame splitting: to unpack he UDP data ,to spun off UDP data from the Loopback data frame, to match whether it is a network performance test frame data, then to read network time parameters calculating delay parameters.

The design of network performance testing software is as follows:

1) To judge whether the address is in the network segment: if it is, then directly send the loopback test frame, start the remote loopback device into the loop state; if it is not, first find the gateway, then send the loopback test frame, tart another remote loopback device into the loop state.

(2) Send transmit path verification test frame, for network access authentication.

(3) Send a test frame, combined with the hardware design, take a network performance test

(4) Send stop test frames, let the loop device to exit the loop state

5 The test results

According to the network composed of 2 household routers, We conducted a series of tests such as throughput, latency, frame loss rate and the back-to-back frame test. The results show that the test results and the general product test results are basically consistent. After the analysis of the results can be seen, short frame network data through a router cost more, leading to throughput smaller. Also found in the router testing, test instruments need to be able to support IGMP simulation, because the router will send out a query command, If there is no response to the query frame, the router will stop the test frame forwarding to the tester of subnet.

6 Conclusion

Using data acquisition system of the front hardware and data processing and analysis system of the background software, in Latency test, by using high precision counter in the FPGA module for clock synchronization and

counting, its timing accuracy is up to 40 ns, which greatly improved the accuracy of time delay test.

In this paper, network tester based on RFC2544 test is presented, with Linux as software platform, and use large-scale FPGA circuit to realize the network performance cross network test. The realization is simple, and can ensure the stable and reliable performance; network interconnection equipment can be completely applied to the actual test by this method. The instrument can be set through the parameters of the default make user conveniently carries on the network performance parameter testing, and through the way of chart make users can intuitively understand the specific network performance. This instrument has been successfully applied to various kinds of communication equipment test site, test scheme and design method for the instrument on network performance test of more high speed, such as 10G network testing also provides reference ideas.

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