A CMOS Analog Baseband for a 5GHzWLAN Direct-Conversion Receiver

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Abstract. This paper describes a CMOS analog baseband circuits for direct-conversion receiver of5GHz IEEE 802.11a. The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA). An active-RC channel selection filter for WLAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. For high linearity, the PGA is constructed with op-amp and resistor based inverting amplifiers. For minimum power consumption, the op-amps employ the current re-using feedforward frequency compensation. The input third-order intercept point (iIP3) is 20dBV at the highest gain mode. Implemented in a 0.18 m CMOS technology, the gain of the programmable gain amplifier (PGA) can be controlled from 2.5dB to 52.5dB with 0.5dB step.

Keywords: WLAN (Wireless Local Area Network), Receiver analog baseband, Channel Selection filter, PGA (Programmable gain amplifier), OP-amp

1   Introduction

RF front end with DCR architecture as shown Fig. 1 can be far simpler ifADC has sufficiently large dynamic range so the channel selection filter can be eliminated. However, the power consumption would become extremely large because ADC is normally a power hungry device. The challenge of analog channel selection filter for WLAN is the fact the channel bandwidth can vary in a very wide frequency range depending on the wireless standard. The simplest approach is to have a channel selection filter whose cut-off frequency is fixed at the value for the wireless standard with widest channel bandwidth among the standards being supported.
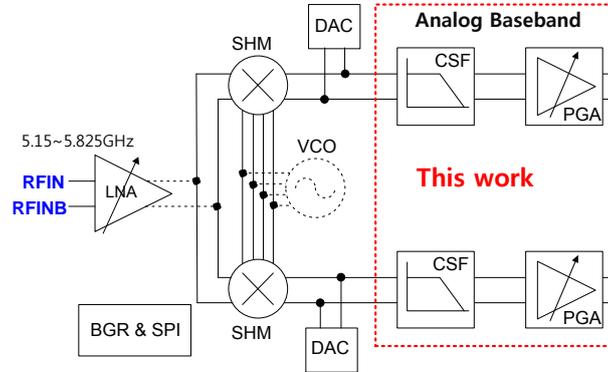
Fig.1. Direct-conversion receiver for 5GHz WLAN

Then, the information is not lost in the channel selection filter even for the other wireless standards. [1]. Several research results on dual-mode analog channel selection filter have been reported [2-3], but to the authors' knowledge there has been no true software definable channel selection filter tunable for multiple wireless standards.

2.1 Channel selection filter
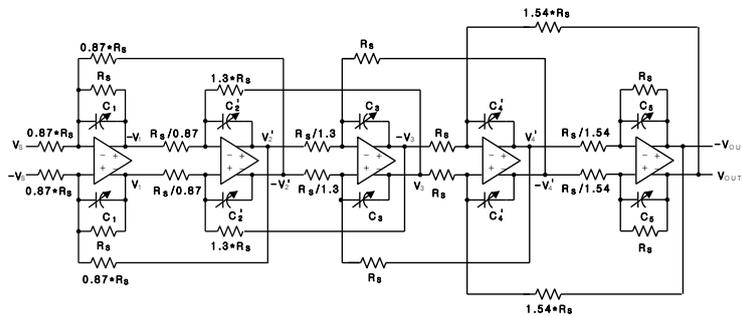
Fig. 2. Fifth-order Chebyshev active-RC filter

For channel selection filtering, a fifth-order Chebyshev active RC filter shown in Fig. 2 is used because it provides relatively large stop-band attenuation with moderate group delay variation within the pass-band [4]. The cut-off frequency of active-RC filter can be tuned by varying the unity-gain frequency of active-RC integrators. The dynamic range of the filter is maximized by scaling the resistor values to have the same maximum signal swing for all internal nodes. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feedforward

frequency compensation scheme [5].The cut-off frequency of CSF can be controlled from 6.3MHz to 20MHz and the stop-band rejection is larger than 41dBas shown in Fig. 3.
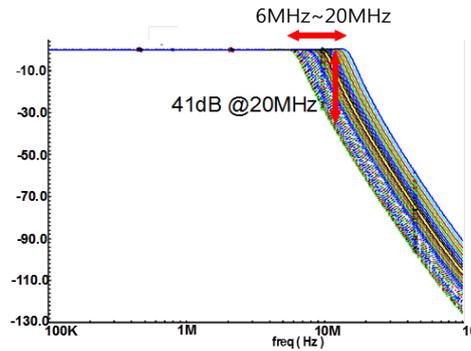

Fig. 3. Frequency response of the LPF for some control code

2.3 Programmable Gain Amplifier

The PGA is placed between the channel selection filter and the ADC. This arrangement relaxes the linearity requirement on the PGA because the out-of-band interferers are attenuated by the filter. But according to the system simulation result, still the linearity requirement on the PGA is very high and thus the op-amp and resistor based inverting amplifiers are used for the implementation of the PGA as shown in Fig.4.
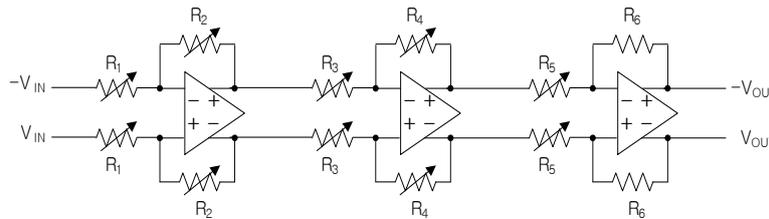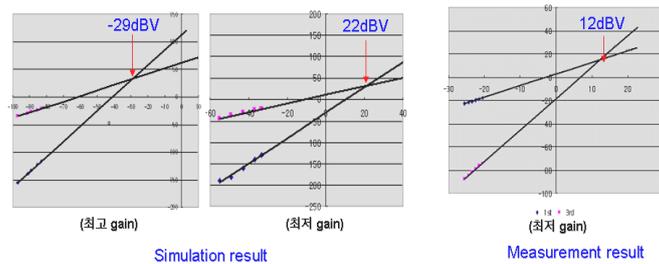

Fig. 4. Programmable Gain Amplifier

It is desired to have high-gain op-amp to get the accurate control of the gain of the PGA. For high-gain op-amp, it is usual to have multi-stage architecture which requires the frequency compensation. The most popular method of frequency compensation is the pole-splitting using a Miller capacitor. With the Miller compensation, however, it is very difficult to achieve high-frequency operation with low supply voltage. Therefore, the feedforward frequency compensation method is used instead [5], [6]. In the feedforward frequency compensation, the phase shift of

the second pole is compensated by the left half plane (LHP) zero generated by the feedforward path as above mention. The PGA has 50dB gain of the control range with 0.5dB step size. In order to achieve the accurate gain value, the resistors are implemented with the array of unit resistance. To minimize the variation and silicon area, high-resistivity poly-Si layer is used for the implementation of the resistors. To minimize the gain error and maximize the linearity, the PGA is constructed with op-amp and resistor based inverting amplifiers.

Fig.5. IIP3 of Programmable Gain Amplifier

The gain error of PGA is smaller than 0.25dB for whole gain control range. The in-band iIP3 is 22dBV and -29dBV, respectively for the highest and lowest gain modes as shown in Fig.5. The input-referred noise voltage is $3.7nV/\sqrt{Hz}$ at the highest gain mode.

5   Conclusion

This paper describes a CMOS direct-conversion receiver analog baseband circuits for 5GHz wireless LAN. The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA). An active-RC channel selection filter for WLAN is described whose cut-off frequency is tunable from 6MHz to 20MHz. This frequency tuning range is sufficient to cover IEEE802.11a (20MHz) including the effect of process, voltage, temperature variations. For wide tuning range, a differential R-2R ladder has been developed which gives widely variable resistance with minimum silicon area. Wide bandwidth operational amplifier (op-amp) is designed to dissipate small power by employing a current re-using feedforward frequency compensation scheme.

For high linearity, the PGA is constructed with op-amp and resistor based inverting amplifiers. For minimum power consumption, the op-amps employ the current re-using feedforward frequency compensation. The input third-order intercept point (iIP3) is 20dBV at the highest gain mode. The input referred noise is $13nV/\sqrt{Hz}$ at the lowest gain mode. Implemented in a 0.18μm CMOS technology, the gain of the programmable gain amplifier (PGA) can be controlled from 2.5dB to 52.5dB with

0.5dB step.

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