A New Low-Power Programmable CMOS Gain Amplifier

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Abstract. This paper presents a new low-power Programmable Gain Amplifier (PGA) to amplify fine various defect signals in steel plates. To detect various inner defects in steel plates, the PGA controls 7-level gains from 6dB to 60dB using the CMOS switches and passive resistors in parallel. It is fabricated using Magnachip/SK Hynix 0.18µm CMOS 1poly-6metal process. The proposed PGA showed excellent gain error of less than 0.18dB, very small die area of 0.016µm² and low power consumption of 0.47mW.

Keywords: Programmable Gain Amplifier (PGA), 0.18µm, CMOS switches.

1 Introduction

The Programmable Gain Amplifier (PGA) is essential to maximize the dynamic output range of the system, and is possible to adjust the gain. It is classified into two types of analog or digital by using a type of programmable gain signal. An analog PGA is generally used with a variable transconductance and resistor, and a digital PGA is more preferable to reduce chip size and power consumption containing a switch to control the digital signal. Recently, the PGA is often controlled and embodied as a feedback loop by Digital Signal Processor (DSP). In this case, it can be used to adjust the programmable gain by using digital control method. The PGA has been used in a variety of fields such as disk drive, hearing aids, optical receiver and wireless communication system, etc. However, the suitable PGA still remains to be the major issues to make affordable commercial systems [1], [2], [3].

In this paper, a new low-power PGA is proposed. This circuit detects various inner defects in steel plates, since it controls gains of 7 levels with 6dB, 12dB, 20dB, 26dB, 32dB, 40dB, and 60dB.

2 PGA Design

Choosing the method to control a gain is an essential at PGA design. The proposed PGA with source degeneration resistor is shown in Fig. 1. It has fully symmetrical structure at differential mode, and sources of transistors M₁-M₂ have an opposite
voltages when two inputs with opposite phases are inserted into the circuit. The amplifier gain can be selected by using a ratio of degeneration or a load resistor. Both sides of the symmetrical structure have the same value of direct current at the source node, and then the gain is adjustable by changing the degeneration resistor. To get higher gain, the value of the total degeneration resistor must be lower, thus it leads to the increment of gain errors. Therefore, to obtain a more accurate and higher gain, the proposed PGA includes gm-boosted source-degenerated differential pair and an additional amplifier stage.

Fig. 1. Proposed PGA

Fig. 2 shows gain adjustment stage for degeneration resistor \((2R_s)\) shown in Fig. 1. The gain of the proposed PGA is determined by the value of degeneration resistor. It consists of 14 MOS switches and 7 resistors to produce various gains such as 6dB, 12dB, 20dB, 26dB, 32dB, 40dB and 60dB, etc. To increase linearity of switch and decrease chip size, we used MOS switches and resistors.

We fabricated using Magnachip/SK Hynix 0.18μm CMOS 1poly-6metal process. It was also used by Cadence Virtuoso for layout and Mentor Calibre for layout verification.

Fig. 2. Gain adjustment stage from switches and resistors

3 Results

Fig. 3 shows transient simulation for the proposed PGA. It is designed by p
providing various gains such as 6dB, 12dB, 20dB, 26dB, 32dB, 40dB and 60dB, etc. The results show average values from 10 times experiments and time variations of within less than ±2%. These values are measured after 40 nanoseconds settling time of the PGA to ensure steady-state value. As shown in Fig. 3, the proposed PGA showed acceptable values of 6dB, 12dB, 20dB, 26dB, 32dB, 40dB and 60dB.

Table 1 shows results of differential-mode gain ($A_{dm}$), common-mode gain ($A_{cm}$) and common-mode-rejection ratio (CMRR) for the proposed PGA. In differential amplifiers with perfect symmetry, each component on the side of one output corresponds to an identical component on the side of the other output as shown in Fig. 1. With such perfectly balanced amplifiers, when $v_{in1} = -v_{in2}$, $v_{out1} = -v_{out2}$. Similarly, pure common-mode inputs (for which differential-mode input, $v_{id} = 0$) produce pure common-mode outputs in perfectly balanced differential amplifiers. Therefore, the ratio $A_{dm}/A_{cm}$ is one figure of merit for a differential amplifier, giving the ratio of the desired differential-mode gain to the undesired common-mode gain. CMRR is defined by the magnitude of this ratio as the common-mode-rejection ratio. As listed in Table 1, the proposed PGA showed excellent CMRR of 83.5dB for 6dB gain and of 137.07dB for 60dB gain, respectively. The PGA also showed very small gain error of less than 0.18dB. The proposed PGA also showed very low power consumption of 0.47mW, small gain error of less than 0.18dB, and very small chip area of 0.016μm² compared to conventional results [3], [4], [5].

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>$A_{dm}$ (dB)</th>
<th>$A_{cm}$ (dB)</th>
<th>CMRR (dB)</th>
</tr>
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<tbody>
<tr>
<td>6dB</td>
<td>5.98</td>
<td>-77.52</td>
<td>83.50</td>
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<tr>
<td>12dB</td>
<td>11.98</td>
<td>-77.49</td>
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<td>20.08</td>
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<td>97.57</td>
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<td>25.94</td>
<td>-77.48</td>
<td>103.42</td>
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<tr>
<td>32dB</td>
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<tr>
<td>60dB</td>
<td>60.18</td>
<td>-76.90</td>
<td>137.07</td>
</tr>
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</table>

Fig. 3. Transient simulation
4 Conclusions

In this paper, we proposed a new low-power Programmable Gain Amplifier (PGA) to detect very small signal from various defects in steel plates. The PGA consisted of differential amplifier stage, buffer stage, CMOS switches and passive resistors. It had perfectly balanced amplifier scheme to reduce input and power supply noises. We fabricated using Magnachip/SK Hynix 0.18μm CMOS 1 poly-6metal process. The proposed PGA showed very low power consumption of 0.47mW, very small gain error of less than 0.18dB, and very small chip area of 0.016μm² compared to conventional results.

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