A 10-bit 100-kS/s Successive Approximation Register ADC with improved Split Capacitor-based DAC

Yeon-Ho Jeong¹, Young-Chan Jang¹

¹Kumoh National Institute of Technology, Gumi, Korea
ycjang@kumoh.ac.kr

Abstract. A 10-bit 100-kS/s successive approximation register (SAR) analog-to-digital converter (ADC) with rail-to-rail input range is proposed for a low power sensor interface. It consists of a time-domain comparator, a split capacitor-based digital-to-analog converter (SC-DAC) and a SAR logic. The time-domain comparator with an offset calibration technique is used to achieve a resolution of 10-bit. To reduce process variation, the value of a split capacitor in the SC-DAC is adjusted to enhance the linearity of the SC-DAC. The proposed 10-bit 100-kS/s SAR ADC is designed using a 0.11-μm CMOS process with a 1 V supply. The power consumption and active area of SAR ADC are 7.49 μW and 0.1056 mm². The maximum SNDR is 60 dB for the analog input frequency of 1.023 kHz when the value of a split capacitor in the SC-DAC is optimized.

Keywords: SAR, Successive approximation register, analog-to-digital converter, offset calibration, linearity.

1 Introduction

Recently, there has been an increase in demand for biomedical-application such as brain wave testing, electromyography and electrocardiography. The analog-to-digital converter (ADC) with low conversion rate is required to convert the sensed bio-signals to the digital form which is analyzed by the digital processor. ADCs with low-power consumption are needed to maximize the battery life. Thus, the architecture of a successive approximation register (SAR) ADC is suitable for bio-medical applications due to its moderate resolution, speed and low-power consumption [1].

2 10-bit 100-kS/s SAR ADC

The proposed SAR ADC with a rail-to-rail input range consists of a split capacitor-based digital-to-analog converter (SC-DAC), a time-domain comparator and a successive approximation register (SAR) logic, as shown in Fig. 1(a). The SC-DAC used in the SAR ADC has a small area than a binary weighted capacitor DAC. It is controlled by the output signals of the SAR logic. The time-domain comparator used
to improve the accuracy converts the voltage difference between the output voltages of the SC-DAC \(V_{DAC+}, V_{DAC-}\) to the time-delay difference. To increase the immunity to noise sources, the time-domain comparator is used with an offset calibration technique.

![Block diagram](image)

Fig. 1. (a) Block diagram (b) timing diagram of SAR ADC

Fig. 1(b) shows timing diagram of the SAR ADC. The conversion requires 12-clock cycles to convert the analog signal to a 10-bit digital code. Thus, a clock frequency of 1.2 MHz is used for sampling rate of 100-kS/s. In the first cycle, the SC-DAC is reset for the initialization of data stored in all the capacitors. In the second cycle, the SC-DAC samples the differential analog input signals. Then the data conversion of 10-bit is performed during the next 10 cycles. The outputs of the SC-DAC approach to the common-mode level of the analog input signal as the conversion process continues.

### 2.1 Split capacitor-based DAC (SC-DAC)

![Split capacitor-based DAC](image)

Fig. 2. Structure of split capacitor-based DAC

For the design of low power, the differential SC-DAC is used in this paper. Generally, the SC-DAC has the advantages of a small area, small total capacitance, and high...
noise immunity. However, this architecture suffers from the mismatch of the split capacitor. It deteriorates the linearity of the SC-DAC. Fig. 2 shows the circuit diagram of the SC-DAC. The SC-DAC consists of two 5-bit capacitor arrays and a split capacitor. The unit capacitance (C) is 150 fF. In this ADC, the value of the split capacitor in the SC-DAC, which is typically 1.0C, is adjusted from 0.9C to 1.2C. According to the process variations, the value of the split capacitor is adjusted to improve the linearity of the SC-DAC.

### 2.2 Time-Domain Comparator

The time-domain comparator consists of a voltage controlled delay converter (VCDC), a time amplifier (TA), a binary phase detector (PD) and a 4-bit FSM, as shown in Fig. 3(a). The VCDC converts the voltage difference between the output voltage of SC-DAC ($V_{DAC+}$, $V_{DAC-}$) to the time-delay difference. Then the time-delay difference is amplified by the TA. Finally, the binary PD senses the polarity of the time-delay difference [2], [3].

![Fig. 3. (a) Block diagram of time-domain comparator (b) circuit of VCDC](image)

Generally, an input offset voltage of a comparator generated due to the process variations such as threshold voltage of a transistor and mismatches in the pattern. In this work, the self-calibration circuit of the time-domain comparator is proposed to eliminate the static input offset voltage by the 4-bit FSM. Fig. 3(b) shows the circuit of the VCDC with the input offset self-calibration circuit which is composed of the pull-up path of the input stage. The offset voltage controlled by one code step is less than 1 LSB. In addition, the input capacitance of the VCDC proposed in this work lower than that of the conventional time-domain comparator.
3 Chip Design and Simulation Results

![Layout of SAR ADC](image1)

![SNDR vs. split capacitor of SC-DAC](image2)

Fig. 4. (a) Layout of SAR ADC (b) SNDR vs. split capacitor of SC-DAC

Fig. 4(a) shows the layout of the designed SAR ADC. The power consumption and active area are 7.5 μW and 0.1056 mm², respectively. Fig. 4(b) shows the FFT simulation result. The maximum SNDR of the SAR ADC with the split capacitor of 1.0C is 60 dB for the analog input frequency of 1.023 kHz.

4 Conclusion

The 10-bit 100-kS/s SAR ADC with a rail-to-rail input signal is proposed for a low power sensor interface. The value of the split capacitor in the SC-DAC is adjusted to improve the linearity of the SC-DAC. The time-domain comparator with an input offset self-calibration circuit is proposed to reduce the analog noise. The designed SAR ADC is designed using a 0.11-μm CMOS process with a 1 V supply. Its SNDR is 60 dB for a 1.023-kHz analog input signal at a sampling rate of 100-kS/s. The power consumption and active area are 7.5 μW and 0.1056 mm², respectively.

Acknowledgments. This work was sponsored by IDEC and ETRI SW-SoC R&BD Center, Human Resource Development Project.

References