Manycore Processor Education Platform with FPGA for Undergraduate Level Computer Architecture Class

Hana Park, Young-Woong Ko, Jungmin So and Jeong-Gun Lee

Dept. of Computer Science, Hallym University,
Chuncheon, South Korea
{hnpark, yuko, js01, jeonggun.lee}@hallym.ac.kr

Abstract. Manycore processor architectures are currently very widely used in almost all computer systems. Furthermore, many computer science department have started to teach parallel programming on manycore system platforms. To best understand the parallel programming on those manycore processors, the classes on manycore processor architecture also have to be provided. However, most current undergraduate computer architecture classes have not yet provided. In this paper, we have design a manycore processor design using a conventional MIPS processor design that is considered as a standard processor architecture model in a traditional undergraduate computer architecture class. Synthesize manycore processor models are developed in 850 lines of Verilog-HDL together with simple parallel applications so students can understand the entire manycore processor design and can learn the basics of the manycore system including underlying communication architecture.

Keywords: Manycore Processor. Computer Architecture, Teaching.

1 Introduction

In a current commercial computing system, manycore processors are major products of many chip manufacturing vendors (e.g., Intel, AMD, nVidia). Quad or hexa-core processors are not only available for high-performance computing but also available for general computing in desktop PC computers. Moreover, those manycore systems are also used in mobile phones. However, in the undergraduate course work of computer science (CS) or computer engineering (CE), there is not yet enough classes for manycore system architecture and programming. In consequence, a manycore processor paradigm is one topic of such mismatches happen between academia and industry. Recently, there have been parallel programming classes in which the lectures on practical CUDA or OpenCL parallel programming languages are provided. However, it seems that there is no enough class on the manycore processor at the viewpoint of a computer architecture. Some advanced chapters of textbooks in computer architecture classes cover the theoretical points of modern high-performance manycore processor architectures, but they do not provide actual design or experimental platform for a manycore processor because its design is more
complex compared with a single cycle processor, a multi-cycle processor and a pipelined processor [1].

2 Related Work

In the literatures of CS and CE educations, there have been many work so far with long history for supporting teaching materials and for establishing course contents that are efficiently deliverable to CS and CE majored university students with better understanding [2].

In [3], the authors have develop a computer-aided teaching package for teaching a processor architecture. The CAT is composed of an assembler and a graphics simulator. In the study, a simple Z80 model is used as a processor model. Similar to [3], a simple processor simulator has been developed as a teaching tool for first-year undergraduates [4]. As a program run on the simulator, the tool shows a snapshot of the processor internals such as register values and program counter. In [5], simple micro-architectures are used as a processor education model for first-year students of computer science with a graphic tool that visualize the operations of the micro-architectures. The authors in [6] have presented a graphical and interactive tools for reduced instruction set computer processor and memory simulator. Through those visualizing tools, undergraduate students can actively learn theoretical concepts covered in computer architecture classes. It is a unique feature of [6] that the simulator can be configured into processors of having many different levels of complexity from a simple processor without caches or pipelines to a highly complex one with caches and superscalar execution. The core idea behind [3, 4, 5, 6] is supporting visualization tools for better understanding of computer architecture operations. In addition to those work, many of similar visualization approaches have been performed so far in the computer science education society.

Another research trend of the processor education in CS / CE is employing an FPGA devices. The programmability of the FPGA is a very fascinating feature in processor design educations because students can make real working processor chip by downloading their designs to the FPGA as opposed to just experimenting software-based simulations. Furthermore, unlike ASIC designs that require at least few months for their implementations, the FPGA device provide a quick verification/test cycle and easy modification capability. Consequently, students can experience all the process of designing a actual product by working on designing, implementing, testing, and debugging processors using a commercial FPGA development boards [7]. Many educational purpose FPGA development boards are available at the University Programs provided by main FPGA chip vendors such as Altera and Xilinx [15, 16]. In [8, 9, 10, 11], an FPGA device has been used as their educational teaching platforms for demonstrating real working processor to students. In [12], the authors have discussed some usage of a FPGA device in teaching processor design class.

Most importantly, students can have much motivations toward their learning for computer architecture because developing a real working processor can be a unique experiences. Our goal of work is to provide the educational processor architecture
model that follows the recent trend of microprocessor market so that students can feel much higher motivation for their learning.

3 Our Manycore Education Platform

In this paper, we develop a synthesizable manycore processor design that can be used in undergraduate-level computer architecture classes. Our manycore processor design is described in Verilog-HDL and it is based on a well-known MIPS processor core [1]. In particular, our synthesizable manycore design is simplified as much as possible for giving students better understanding on manycore processor internals, while the communication architectures, such as "shared memory structure", are being described. The communication architecture are currently a core design issue in a camera usb modern manycore design. The manycore model has been synthesized successfully with the Altera Quartus II CAD tool and implemented and tested on a commercial field programmable gate array (FPGA) development platform called a DE2-70 FPGA board that is developed by the Altera Corporation.

We expect that the manycore processor architecture model is used as educational platform for teaching practical experiments of manycore processor designs at the undergraduate computer architecture classes.

References
