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Low-power Design of Adiabatic Dynamic CMOS Logic using Parasitic Capacitance of 0.18μm Standard CMOS Model

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Abstract. In this paper, the influence on the load capacitance value of the adiabatic dynamic CMOS logic (ADCL) is examined. The adiabatic operation and reduction effect of power consumption are confirmed using LTspice with 0.18μm standard MOS model. Furthermore, the 3-bit digital PWM using ADCL without voltage holding capacitance (C_S) was simulated for the organic light emitting diodes (OLEDs) dimming systems. The power consumption of the ADCL digital PWM without C_S for all bit patterns decreased by 52.3 % compared to that of the ADCL PWM with C_S.

Keywords: adiabatic dynamic CMOS logic, voltage holding capacitance, parasitic capacitance, low-power design, digital PWM, OLED lighting system

1 Introduction

Environmental development for deep sleep has been studied using analysis results of the big data about parameters in the bedroom; temperature, humidity, brightness of illumination etc. [1]. The organic light emitting diodes (OLEDs) which are the closest to natural light have been widely used for illumination of the bedroom and are dimming using analysis results of the big data [2]. Therefore, a low-power dimming part is required for OLED system [1].

The adiabatic dynamic CMOS logic (ADCL) needs a load capacitance (C_L) to maintain the output voltage and prevent backflow of the current. However, power consumption is increased by the C_L. Recently, the miniaturization of integrated circuits is progressing year by year, and it is expected that the voltage holding capacitance (C_S) can be reduced and removed in ADCL because the power supply voltage is lowered and the parasitic capacitance (C_P) exist on transistors.

In this paper, the influence on the load capacitance value of the ADCL is examined. Furthermore, the adiabatic operation and reduction effect of power consumption are confirmed using 0.18μm standard CMOS model.

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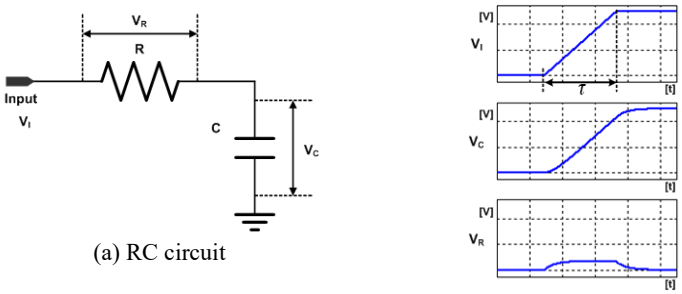
2 Adiabatic Logic

2.1 Adiabatic Charging

In order to minimize the power dissipation, adiabatic charging is one of the promising candidates with AC power, which has a slower rising/falling time than charge/discharge time constant [3][4].



(a) RC circuit

(b) adiabatic charging

Fig. 1. Operation of the RC circuit

Figure 1 shows the adiabatic charging operations at a normal RC circuit. In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are [1][4]

$$v_I(t) = \frac{V_I}{\tau} t\left[u(t) - u(t-\tau)\right] + V_I\left[u(t-\tau)\right] \tag{1}$$

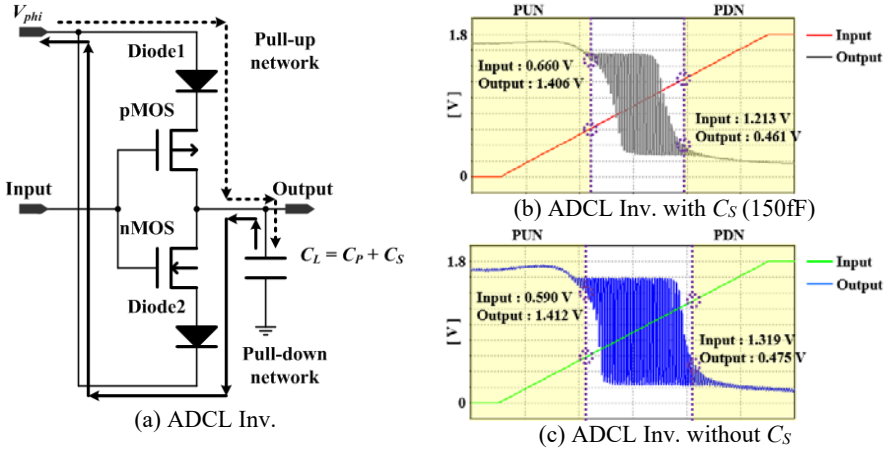
$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1 - e^{-\frac{t}{CR}}\right) - \left(1 - e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right] \tag{2}$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1 - e^{-\frac{t}{CR}}\right) - \left(1 - e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2 \tag{3}$$

There is an influence of power consumption depending on the size of the load capacitance as shown in Eq.3.

2.2 Adiabatic Dynamic CMOS Logic (ADCL) using Parasitic Capacitance

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging/discharging as it is applied to the CMOS logic. In this conventional circuit, the C_L is the C_P and the C_S [1][4]. It is possible to maintain the output voltage using only the C_P of 0.18μm standard COMS model without C_S as shown in Fig 2(c).



(a) ADCL Inv.

(b) ADCL Inv. with C_S (150fF)

(c) ADCL Inv. without C_S

Fig. 2. ADCL Inverter

3 3-bit Digital PWM using ADCL without C_S

The 3-bit digital PWM using ADCL without C_S was simulated using LTspice with 0.18μm standard MOS model. The DC power, AC power and clock were 1.8V, 33kHz triangular wave, 3kHz, respectively. Figure 3 shows simulation results. The simulation confirmed adiabatic charge/discharge using parasitic capacitances of 0.18μm standard CMOS model.

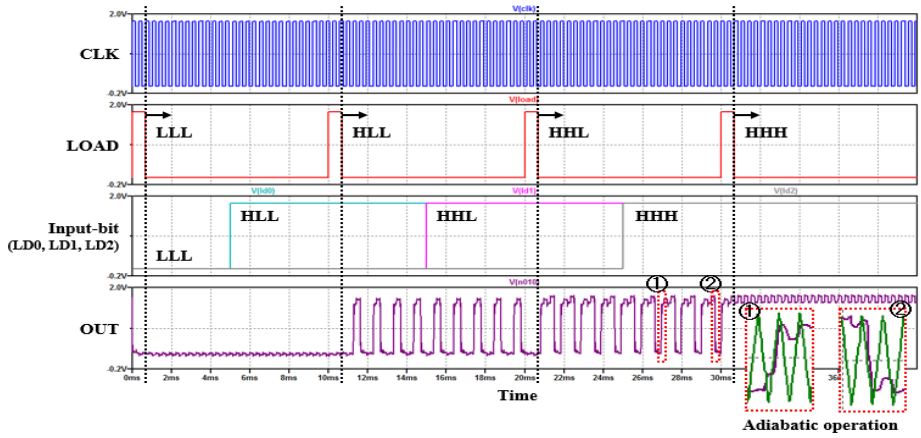


Fig. 3. Waveform of 3-bit digital PWM using ADCL without C_S

The power consumption of the ADCL digital PWM with C_S and without C_S were compared, as shown in Fig. 4. The power consumption of the ADCL digital PWM

without C_S for all bit patterns decreased by 52.3 % compared to that of the ADCL PWM with C_S.

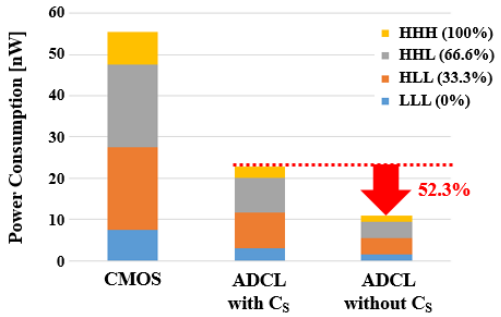


Fig. 4. Comparison of the power consumption

4 Conclusion

The influence on the C_L of the ADCL was examined and the adiabatic operation and reduction effect of power consumption were confirmed using 0.18μm standard CMOS model. The power consumption of the ADCL digital PWM without C_S decreased that of the ADCL PWM with C_S. This shows the potential of the ADCL PWM in future low-power and miniaturization OLED dimming systems for analysis results of the big data about parameters in the bedroom.

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