Reversible Computing in QCA Based on Toffoli Gate

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Abstract. Reversible computing is the procedure to future computing technologies, which all occur to use reversible logic. A reversible logic gate has the capability to decrease the power dissipation which is the main requirement in low power Very-large-scale integration design. It has vast applications and related to other emerging technologies such as low power CMOS, quantum computation and nanotechnology. Because reversible logic promises extremely low power consumption with high density and operating frequency. The main target of designing reversible logic is to reduce quantum cost, the extent of the circuits and the number of garbage outputs. The purpose of this paper is to present a new design of reversible logic 3x3 Toffoli gate with low complexity. The proposed design leads to the reduction of power consumption compared with previous logic circuits.

Keywords: Quantum-dot cellular automata, Reversible logic, Toffoli gate, Nanoelectronics.

1 Introduction

In the last decade, reversible computation has been getting considerable attention in the manufacturing low power consumption technologies. One of the important issues in the modern computational system is managing power dissipation. The cause of the power dissipation issue depends on that the number of bits lost during the computational process. In fact, zero and one represent any number in the digital computer. Inwardly, computers consist of millions of gates which execute logic operations. These logic operations are mostly performed as irreversible computation.

It is more understandable as an example Pentium IV: if every transistor out of the forty million transistors in the processor dissipates heat with relatively 1 GHz frequency, then approximately 0.05 watt power is consumed. It means that the processor works at approximately 300 K temperature. According to Moor's law, the calculated numbers will increase exponentially. If this current trend continues, an unendurable amount of heat is generated by computer systems [1]. Hence, the reversible computation can solve these problems.

The reversible logic operation does not erase binary information. Therefore, there is no heat by the concept. Moreover, the system can operate in a backward direction. It allows us reproducing the inputs from the outputs, so it is called reversible. In the late
70s, Toffoli and Fredkin discovered reversible logic. After that, several other the reversible gates also have been proposed such as, Feynman gate, Peres gate, Margolus gate and others [1, 2].

In this paper, we present the design of Toffoli gate based on QCA. Quantum-dot cellular automata (QCA) is a new paradigm that can be alternative nano technology to the transistor based CMOS technology. It has several extremely advantages: low power consumption, high speed switching and also nano dimension size circuits over transistor based technology. Computation method of this technology is based on cellular automata. Information is represented by the state of the QCA cell which is basic element of the technology. QCA is also one the model of the quantum computation that has getting developed day by day. Our work in this paper is to implement the efficient design of Toffoli reversible gate in QCA. It is one of the extensively used reversible logics, so low complexity design can be proper to construct reversible QCA ALU [2].

2 Related Work

2.1 QCA

A quantum cell is main element of QCA. Each QCA cell consists of four quantum dots with two free electrons. The positions of the electrons denote the logic state. There are two position in QCA as cell polarization \( P = +1 \) and \( P = -1 \) shown in Figure 1(a). Resulting either polarization \( P = +1 \) to introduce binary ‘1’ and \( P = -1 \) to introduce binary ‘0’. When two cells are getting nearly together, due to coulombic interaction the cells accept on the same polarization [2, 3]. Binary information is propagated using cell states [4].

![Fig. 1. a) QCA cells with two different polarizations, b) QCA 3-input majority gate](image)

Majority gate and inverter are essential building parts of this technology. Three input majority gate is conventional majority gate and it equation is \( M(A, B, C) = AB + AC + BC \). The function of the majority gate is to generate three inputs and eventually to get desired output. It is composed of five QCA cells: three input cells (A, B and C), one output cell (M(A,B,C)) and one inside cell. It can be implemented by five cells arranged in a cross as illustrated in Figure 1(b) [5]. Any digital logic circuit is represented by logic AND or OR operation. If one of the inputs is set to polarization minus one, logic AND operation can be constructed in the majority gate. Similarly, one of the inputs is
set to polarization plus one, logic operation OR is constructed. Hence, any complex logic circuits can be implemented from logic OR and logic AND gates respectively as:

\[ A + B = M(A, B, 1); \]
\[ AB = M(A, B, 0); \]

QCA wire is constructed with plural numbers of cells. By QCA wire information is transfer cell by cell since electrostatic interaction. By placing cell with their edges contact sequentially, simple QCA inverter is implemented. It is used to invert transferring signal from one form to invers form, as shown in Figure 2(b). In this technology, wire crossing is complicated point in the crossing two different wires. There are two types of wire crossing, such as coplanar wire crossing technique and stereoscopic wire crossing, namely multilayer form, as illustrated in Figure 2(a). For getting strong signal strength, multilayer wire crossing is more proper than coplanar crossing which is composed of rotated cells [5, 6]. However, there is another efficient form of coplanar wire crossing and it is based on QCA clocking technique [5,6].

![Fig. 2](image)

*Fig. 2.* a) Typical wire-crossing techniques coplanar and multilayer crossover, b) QCA inverter structures robust inverter and simple inverter.

QCA circuits use clock system for manage data transfer and synchronize. The main advantage of QCA clock system is to provide the power to run the circuit because the quantum cells are not exterior source for powering. QCA clock system makes use of four phases clocking for regulating cells. It is realized by the steps: switch, hold, release and relax phases, as demonstrated in Figure 3. As a mentioned before, QCA clocking can be utilized in the wire crossing. QCA circuit is divided with four clock zones. The zero zone(zone-0) cannot meet with zone two(zone-2), similarly, zone one(zone-1) cannot meet with zone three(zone-3). By the concept, wire crossing can be realized in QCA circuit easily[7,8].
2.2 Toffoli Gate

The number of inputs and the number of outputs are equal to in reversible logic circuits with one-to-one mapping between them. Number of 1’s in the inputs is equal to the number of 1’s in the outputs. If the output is given, then it is possible to recover the input [8]. Therefore, it is called reverse logic. The first reversible logic gate is 3x3 Toffoli gate and it is also known as controlled controlled-not. Its equations as follow: P=A, Q=B, R=AB\oplus C. Figure 4 illustrates the block diagram of the gate and its truth table, respectively [6, 7, 8].

![Fig. 3. Clocking scheme](image)

![Fig. 4. a) block diagram of Toffoli gate b) trust table of Toffoli gate](image)
3 Proposed design of Toffoli Gate

The proposed new design of Toffoli gate composed of one 3-input majority and one XOR gate. Figure 5 shows the schematic diagram and QCA implement of Toffoli gate, respectively. This layout consists of 46 quantum cell and using 4 clock phases. The structure is occupied by 0.058 $\mu$m² total area with low complexity. In this design, single layer wire crossing which is based on QCA clocking is used. It can lead to compact circuit and realization of the design in complex circuit architecture can be more proper.

Fig. 5. The schematic diagram and QCA implement of Toffoli gate

We have used QCADesigner that is efficient simulation tool for QCA circuit. Configuration of the tool is set to bistable approximation. The simulation waveform of the design is demonstrated in Figure 6 and it confirms that all functionality of the presented gate works well with strong signal strength. In the simulation result, red rectangle shows binary sequence of the truth table of the Toffoli gate and it matches relatively with original one, as illustrated in Figure 4(b).
Several prior works are discussed about Toffoli gate in QCA technology. Some of them are misalignment to standard form of the reversible structure, such as less complexity design [10, 11] is used less cells in his design, but one of the outputs is placed inside of the structure. In the design [9], all construction way is by the rule of reversible construction, but with more cell count and bigger occupation area. Table 1 shows comparison of the typical circuit with our circuit. Our design has achieved improvements in terms of used cell count, total area as well as with regular construction way.

Table 1. Comparison result of Toffoli gates

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Cell count</th>
<th>Total area (µm²)</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toffoli gate[9]</td>
<td>75</td>
<td>0.136</td>
<td>4</td>
</tr>
<tr>
<td>Toffoli gate[10]</td>
<td>57</td>
<td>0.060</td>
<td>3</td>
</tr>
<tr>
<td>Proposed design</td>
<td>46</td>
<td>0.058</td>
<td>4</td>
</tr>
</tbody>
</table>

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4 Conclusions

In this paper, less complexity reversible Toffoli gate has been presented in QCA technology. All functionality and correctness have been evaluated using QCADesigner tool and the obtained results also have been compared with other existing works. The comparison table shows that the proposed design has achieved a large amount of improvements on the space complexity such as the number of cells and total area. Actually the
latency of the circuit has been already small enough so that we focused on the space and construction problem. Our circuit has excellent regularity and expandability so that it could be an efficient component within configuration of a circuit.

References