Efficient Motion Estimation Algorithms for High-Performance HEVC Encoder

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Abstract. In this paper, we propose an efficient algorithm for computing architecture for high-performance Inter Prediction SAD encoder. HEVC Motion Estimation(ME) of the Inter prediction is a process for searching for the currently high prediction block PU and the correlation in the interpolated reference picture in order to remove temporal redundancy. This paper proposes a new algorithm which reduces the computational complexity by reusing the 4x4 SAD operation in full search to reduce the amount of calculation and computational time of the Inter Prediction. The proposed algorithm is applied to an HEVC standard software HM16.12. There was an improved operational time of 61% compared to the traditional full search algorithm, BDBitrate was decreased by 11.81% and BDP\text{SNR} increased by about 0.515%

Keywords: HEVC, Inter Prediction, SAD

1 Introduction

Recently video codec HEVC has significantly increased in various coding structures and various techniques have improved prediction calculation complexity compared to H.264/AVC in accordance with [1]. New techniques of HEVC motion prediction methods take into consideration the current characteristics of the original pixels and sub-pixels in the process of comparing the correlation of the PU and the reference block in order to generate the current frame and the most similar prediction frame measurement using SAD (Sum of Absolute Difference). However, in the case of Full Search for inter prediction, there is a high amount of computational and calculation time because the SAD operation is performed on all block sizes of the PU(original) from 64x64 down to 4x4 and repeat the SAD calculation for the reference search area.

In this paper, we propose a new algorithm that reduces the amount of calculation and computational time of the SAD operation for high-performance HEVC Inter Prediction.
2 HEVC Inter Prediction

Motion estimation (ME) of the inter prediction is a process of comparing the correlation between the reference PU and current PU by the encoder for similarities. This correlation measurement determined by the SAD and is shown in formula 1:

\[
SAD(i, j, k, l) = \sum |B_{cur}(i, j) - B_{ref}(k, l)|
\]  

(B\textsubscript{cur} is the current block, B\textsubscript{ref} is the reference block, \{i, j\} represent current PU location and \{k, l\} represent reference PU location. Motion estimation of the integer pixel is selected by the reference block that minimizes the absolute value of the difference of the current block and the reference block, selecting a prediction block in the end.

After performing ME, the encoder produces a reference picture index, reference picture list, motion vector signal and quantization coefficient information which are transmitted to the decoder. In the decoder, the peripheral information received from the encoder generates the same prediction block as the encoder using the quantized residual signal to compute a motion compensation step [2]. Figure 1 illustrates the motion estimation process.

![Fig. 1. Motion estimation process](image)

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3 Proposed SAD algorithm

In the proposed SAD algorithm, the maximum CU block size is 64x64. A 4x4 block size is utilized in the storage of the SAD operation results for re-use in all SAD operation to determine the optimal size for PU mode. The original full-search SAD algorithm computes all possible values for the search range. Therefore, the SAD operation is performed repeatedly causing redundancy and increasing the complexity which consistently lowers the overall encoding time.

In order to reduce the repeatability of the SAD operation process, the proposed SAD algorithm stores the SAD value in a 4x4 block size for further reuse. The sum of the SAD result of the four 4x4 blocks as shown in Figure2 is the same as the SAD value of the 8x8 block and thus the result of the four 8x8 blocks create the same output as the SAD value of the 16x16 block. In this regard, all 23 categories as shown in the PU table for the MAX CU of 32x32 block size can be achieved via the 4x4 unit SAD operation.

![Figure 2. Method of block re-use](image)

Figure 3 shows the flowchart of the proposed algorithm.

![Figure 3. Proposed algorithm flowchart](image)
XCheckRDCostMerge2N×2N to calculate the RD-Cost for skip and Merge. Then, when 2N×2N SAD operation is performed instead of calculating RD-Cost in order of PU split mode such as 2N×2N, N×N, N×2N, 2N×N, etc. SAD result is stored in the 4×4 unit memory. Next, in order of N×N, N×2N, and 2N×N PU mode, memory indexes of the corresponding area are called in order to obtain the result value. In the process of calculating the RD cost for the last AMP (Asymmetric Motion Partition) partition, the index of the corresponding area is called to determine the optimal PU mode.

4 Performance Comparison

The performance of the proposed SAD algorithm was compared to the standard software HM-16.12. The proposed algorithm was tested on a variety of resolutions by evaluating QP values 22, 27, 32 and 37 for each image class.

Table 1. PU block sizes in Inter prediction

<table>
<thead>
<tr>
<th>Sizes</th>
<th>Proposed</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BDPSNR</td>
<td>BD bitrate</td>
</tr>
<tr>
<td>4k</td>
<td>0.335</td>
<td>-8.01</td>
</tr>
<tr>
<td>Avg</td>
<td>0.515</td>
<td>-11.81</td>
</tr>
</tbody>
</table>

Table 1 shows the experimental results for the proposed algorithm. There was an average increase of 61% in encoding time compared to standard HM.16.12 from equation (2). In addition, BD-PSNR increased by 0.515 and BD-Bitrate reduced by 11.81.

5 Conclusion

This paper describes a new algorithm that reduces the amount of calculation and computational time of the SAD operation for high-performance HEVC Inter Prediction. The proposed scheme showed a significantly better result than HM.16.12 standard software in all performance parameters applied that is encoding time (computational intensity), BD-PSNR and BD-Bitrate. The SAD algorithm proposed also has the advantage of minimizing the operational time in hardware module design. However, extra hardware is needed for storing the 4x4 SAD operation results and further studies needful for effective memory management.
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