Miniaturized Design of Control Block of PWM using ADCL for OLED Dimming System

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Abstract. The environment development for deep sleep has been studied using analysis results of the big data about parameters in the bedroom. The organic light emitting diode (OLED) illuminations of the bedroom are dimming using analysis results of the big data. Therefore, a low-power and compact design of dimming part is required for OLED system. In this paper, the miniaturized control block of the clock cut-off circuit was designed using De Morgan’s laws with adiabatic dynamic CMOS logic (ADCL) digital 3-bit PWM. The designed control block pauses the D-fls after cutting off the clock at both dimming 0 % and 100 % of PWM output. The operation of control block is confirmed by post-simulation using hspice with Rohm 0.18um standard CMOS model. As a result 10 transistors of the miniaturized control block were reduced.

Keywords: clock cut-off circuit, miniaturization, adiabatic dynamic CMOS logic, digital PWM, SSL dimming system

1 Introduction

Recently, personal health check and care is increasing using wearable device, ubiquitous device and internet of things (IoT) service [1]. Moreover, environment development for deep sleep has been studied using analysis results of the big data about parameters in the bedroom; temperature, humidity, brightness of illumination etc. The organic light emitting diodes (OLEDs) which are the closest to natural light have been widely used for illumination of the bedroom and are dimming using analysis results of the big data [2]. Therefore, a low-power and compact design of dimming part is required for OLED system [3].

In this paper, the miniaturized control block of the clock cut-off circuit is designed using De Morgan’s laws with adiabatic dynamic CMOS logic (ADCL) digital 3-bit PWM for OLED dimming system.
2 Adiabatic Logic

2.1 Adiabatic Charging

During a sudden transition between high and low levels of the input voltage, a load capacitor cannot be charged and discharged immediately. Power dissipation occurs by the resistive component of the logic circuit in the conventional CMOS logic because this logic circuit uses a constant voltage; DC power supply. To minimize the power dissipation, adiabatic charging is one of the promising candidates with AC power, which has a slower rising/falling time than charge/discharge time constant [4][5].

Fig. 1. Operation of the RC circuit

Figure 1 shows the operations at a normal RC circuit with a DC signal, adiabatic charging, and unsynchronization [11-15]. In the case of the DC signal at the input signal, the energy dissipation occurred at the load R until the end of charging at the load C, as shown in Fig. 1(b). On the other hand, in the case of the AC signal as the input signal, adiabatic charging and little power dissipation are shown in Fig. 1(c). The region of adiabatic charging decreased with increasing $\phi$ of the AC signal, as shown in Fig. 1(d) [5].

2.2 Adiabatic Dynamic CMOS Logic (ADCL)

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging/discharging as it is applied to the CMOS logic. In this circuit, because the output voltage of the ADCL gate is synchronized with the power supply, $V_{\phi}$, the operating speed of the ADCL gates is determined by the frequency of $V_{\phi}$ [6][7].

3 Miniaturization of Control Block and Simulation Results

Unnecessary operation at both dimming 0 % and 100 % of PWM output results in power consumption. The designed clock cut-off circuit pauses the D-fls after cutting
off the clock at both input-bit LLL (0 %) and HHH (100 %), and performs normal operation of the D-fls at other case.

Figure 2 shows the miniaturized control block of the clock cut-off circuit using De Morgan’s laws with ADCL digital 3-bit PWM. The up-level D-latch was used to output the logic level of the SW and PO by the input-bit if the load is reset but to remain at the logic level of the pre-state if the load is set. Table 1 lists the elements. Compared to the control block of Ref. [3], 10 transistors were reduced.

Table 1. Comparison of the elements

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<th>Ref. [3]</th>
<th>This paper</th>
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<tr>
<td></td>
<td>Logic gate</td>
<td>Tr.(ea)</td>
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<tr>
<td>D-latch</td>
<td>3ea</td>
<td>54</td>
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<tr>
<td>Inv.</td>
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<td>18</td>
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<tr>
<td>OR3</td>
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<tr>
<td>Total</td>
<td>94</td>
<td>Total</td>
</tr>
</tbody>
</table>

Figure 3 shows layout of the miniaturized control block using Rohm 0.18μm standard CMOS model. Layout area of the miniaturized control block is 2,235.3μm², which decreased by 7.5 % compared to that of the control block of Ref. [3].
The miniaturized control block was simulated using hspice with Rohm 0.18um standard CMOS model. Figure 4 shows the simulation results. The post-simulation confirmed that the SW is low level at both input-bits HHH and LLL. Moreover, the PO is a high level at input-bit HHH.

4 Conclusion

In this paper, the miniaturized control block of the clock cut-off circuit was designed using De Morgan’s laws with ADCL digital 3-bit PWM. Layout area of miniaturized control block was 7.5 % lower than that of the control block of Ref. [3], because 10 transistors were reduced. The operation of control block is confirmed by computer simulation. This shows the potential of the optimized ADCL PWM in future low-power SSL dimming systems.

Acknowledgments. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

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