An Approach to Formal Verification for AMS SoC

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Abstract. This paper proposes a new scalable approach to formal verification (SFV) for AMS SoC designs. Induction rules defined in computer symbolic algebra system Maple are followed to extract representation of property of AMS SoC, constraints solving is performed to formally verify the correctness of the system with respect to its given property. With an AMS description and a set of properties, SMT based model checker is applied to validate if the given system has a certain property. The proposed methodology is applied on a tunnel diode oscillator. Experimental results for a benchmark and a tunnel diode oscillator demonstrate the effectiveness of the approach. The proposed method is scalable to other AMS system using its adoption of language VHDL-AMS as description tool.

Keywords: AMS SoC, formal verification, Maple

1 Introduction

Nowadays with the ever-increasing complexity of System-on-Chips (SoC), analog and Mixed-Signal (AMS) designs are becoming more and more complicated in electronic devices. Analog devices are small but may cause a lot of problems, it is reported that 20% - 80% fault comes from analog circuits. Moreover our ability to understand complex systems grows slower than our ability to assemble them; verification of analog circuits is becoming a bottleneck for AMS design and plays an important role in today’s industrial design flow.

The verification of AMS designs concerns the correct functionality in addition to checking whether an AMS design is robust with respect to different kinds of inaccuracies like noises, nonlinearities, etc. However, due to the fact that time-to-market is shrinking, re-spins during postsilicon phase incur a huge cost in terms of time and money, additionally formal verification meets with a couple of issues, i.e., interaction between digital and analog blocks are extremely complicated and simulation for AMS design can be in weeks, it is late when bugs are found. It is
significant and time-urgent for verification researchers and engineers to provide high-quality designs to reduce test costs and enhance development efficiency.

Techniques of simulation and test for formal verification of AMS designs have been tapped in [1]. In the past thirty years, formal verification has been applied for digital hardware system and software system. As a technology to overcome the limitation of traditional simulation techniques, formal verification has been suitable for and utilized verification for AMS system [4]. Hybrid semi-formal techniques, which combine simulation and formal methods, have been exploited, where the logic model is used to analyze simulation structure. Linear transfer equation is proposed in [5] to describe the two designs for analog system for model checking. The proposed method bases on bi-linear transfer and transfer function is discrete to z domain. Therefore the design can be expressed as discrete-time component, and be encoded as finite state machine like binary decision tree.

This paper proposes a scalable method for verification of AMS SoC. First, abstractions of circuit behaviors using exhaustive algorithm is formulated for reachability analysis. For one running process with initial status and input signals given, model checking searches the whole state space to demonstrate that all the reachable states meet predefined specifications.

2 The proposed algorithm SFV

Figure 1 shows the flow of formal verification for AMS SoC. Model for the original system is established, and then polyhedral partition and reachable set approximation are performed. The original system is transformed into finite state transitional one. Actions based temporal model is adopted for satisfactory modular theory (SMT) based model checking to judge if the system meets the specifications. The property of AMS design is written as $\Phi$ in programming languages VHDL-AMS, and the AMS system is formally represented as $M$. A model checking algorithm determines whether a mathematical model of a system meets a specification. Or formally, given a model $M$ of an AMS SoC and a property $P$, $\text{check}_{M} P$, i.e., check if $P$ holds in the model $M$. 


The proposed method searches for a counter-example for a given property verified against the design model $M$ for bounded number of verification steps. If a concrete counter-example is found, then refinement is performed to repeat the verification, otherwise, it needs to increase the number of steps until property validation is carried out. Generally speaking, the verification is not complete because of time and memory limitations. To overcome this problem, we observed that under certain conditions and for some classes of specification properties, the verification can be complete if we complement the BMC with other methods such as abstraction and constraint based verification methods. To test and validate the proposed approaches, we developed a prototype implementation in Maple and we targeted AMS design like tunnel diode oscillator for the tests of the proposed approach.

Tunnel diode oscillator shown as Figure 2 is taken for research target. For some range of voltages, the current of tunnel diode oscillator decreases with increasing voltage as shown in figure 3. More specifically, when a small forward-bias voltage is applied across a tunnel diode oscillator, it begins to conduct current. As the voltage increases, the current increases and reaches a peak value. If the voltage increases a little bit, the current virtually starts to decrease until it reaches valley value.
3 Experimental Results

For the tunnel diode oscillator, it needs 32 separate regions to model the oscillatory and non-oscillatory behaviors. The property is verified when the current $I$ is between 0.45 and 0.55 mA and voltage $V_c$ is between 0.4 and 0.47 V. As expected, the property is verified with $R = 200$ in 13.01 s after finding 16512 state sets, and the property is not verified when $R = 242$ in 0.57 s after finding 1895 state sets. The verification using the HyTech tool is realized. HyTech can complete analysis with less precision, at the expense of no longer producing oscillating behavior. The proposed approach completes the verification work on the tunnel diode oscillator in 10.39 s, and outperforms model checker HyTech which consumes 68.4 s. This indicates that our method can provide drastic performance improvement over two other methods with no loss in verification accuracy.

Table 1 shows the verification results for HyTech [6], LHPN [7] and the proposed method. The same parameters as [8] are used for the experiment. The initial current and voltage are $I \in [0.4, 0.5]$ mA, $V_c \in [0.4, 0.5]$ V.

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<tr>
<td>Instance</td>
<td>Time(s)</td>
<td>Verified?</td>
<td>Time(s)</td>
</tr>
<tr>
<td>tunnel diode oscillator</td>
<td>68.4</td>
<td>N/A</td>
<td>13.01 ($R=200\Omega$)</td>
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<td>(oscillatory)</td>
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<tr>
<td>tunnel diode oscillator</td>
<td>n.r.</td>
<td>N/A</td>
<td>0.57 ($R=242\Omega$)</td>
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<td>(Non-oscillatory)</td>
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The proposed verification method mainly deals with modeling for oscillating behavior and non-oscillating behaviors of tunnel diode oscillator using 32-bit discrete regions. When $R=200\Omega$, LHPN model uses 13.01 s for property verification. 16512 state sets are found in 13.01 s when $R=242\Omega$, 1895 state sets are found in 0.57 s when $R=242\Omega$. We failed to use tool HyTech for verification because of overflow errors. HyTech model checking accomplishes oscillating property checking for tunnel diode oscillator.
oscillator within 68.4 s, however the proposed method only takes 11.57 s, hence obtains higher efficiency than that in [7].

4 Conclusion

This paper presents a scalable approach to formal verification of dynamic property for AMS designs: SFV. The proposed method is applied on tunnel diode oscillator for formal verification of AMS SoC. An AMS SoC and a set of properties are expressed in VHDL-AMS, then SMT based model checking is adopted to validate if the properties hold in the given model for the design, if the properties are satisfied then the algorithm terminates otherwise the counter-example are found. Experimental results demonstrate the effectiveness of the proposed method. The proof for stability and oscillatory state of tunnel diode oscillator has been conducted respectively under two sets of parameters.

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References