Abstract: Thermal-aware Floorplan Schemes for High-Performance 3D Multi-core Processors

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Abstract

As integration densities continue to increase, interconnection delay has become the bottleneck in improving the performance of multi-core processors. 3D integration technology can be a good solution for reducing the interconnection delay in the multi-core processor. In 3D multi-core processors, multiple cores are stacked vertically and the cores on different layers are connected by direct vertical through-silicon vias. Therefore, 3D multi-core processors can reduce the interconnection delay and power consumption significantly compared to 2D multi-core processors. However, the 3D design technique cannot be practical without proper thermal solutions, because the 3D architecture causes severe thermal problems due to high power density in the chip. To solve the thermal problems in the 3D multi-core processor, this paper proposes the thermal-aware floorplan techniques to reduce the peak temperature in the 3D multi-core processor. According to our experimental results, the proposed techniques alleviate the thermal problems in 3D multi-core processors significantly, leading to the improved performance, energy-efficiency and reliability.

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