A New Low Power Four Quadrant Analog Multiplier

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Abstract. In this paper a low power CMOS four quadrant analog multiplier is presented. The proposed topology is in a way that the output is taken as fully differential signals for achieving more output range. The proposed topology is simulated using HSPICE simulator in 0.18 m standard CMOS Technology with 0.15V supply voltage. The simulation results show that the total power consumption is 444.5pW.

Keywords: CMOS circuits, Low power, Analog multiplier, four quadrants.

1 Introduction

An analog multiplier is a device having two input ports and an output port. The signal at the output is the product of the two input signals. Signals can be currents or voltages due to the demand [1]. As analog multiplication is important in many operations so it has a wide of applications in many fields like adaptive filters, equalizer, modulators, automatic gain controlling, artificial neural networks [2, 3, 4], image processing and medicine [5]. These days, the electronic society is faced with orders in relation to low power dissipations [4, 6].

The initial multiplier topologies were proposed by Gilbert [7]. There are many works that has presented a variety of four quadrant multiplier circuits for low power applications. Among them a possible way to achieve a low power dissipation topology is to use MOSFETs in weak inversion region and the other way is to drive them in bulk terminals. In this paper, a CMOS low power four quadrant analog multiplier is presented. We use differential inputs and we have differential outputs too.

The rest of this paper is organized as follows: section 2 briefly describes the research background. Section 3 presents the proposed multiplier. Simulation Results are presented in section 4. Finally, the paper is concluded in section 5.
2 Background

With respect to the operation of a MOS device in weak inversion, relative equations are as follows:

\[
I_{DS} = I_{D0} e^{\frac{-V_{DS}}{kT}} e^{\frac{-\eta (V_{GS} - V_{TH})}{kT}} \left[1 - e^{\frac{-V_{DS}}{kT}}\right] \tag{1}
\]

Eq. 1 is the drain to source current of MOS, in which

\[I_{D0} = I_e e^{\frac{V_{TH}}{kT}},\]
\[I_s = 2 \eta \beta u T \eta, \eta = \frac{e^{RT}}{q},\]

\(\eta\) is the sub-threshold slope factor and is between 1 and 2 [8,9],

\(\beta = \mu C_o \frac{W}{L} V_E,\)

and \(V_E\) is the early voltage that is nearly 10 V.

The exponential function in this topology defines as a current mirror which is biased in bulk terminals [10].

3 The Proposed Architecture

The utilized four quadrant multiplier is shown in figure 1.

![Fig. 1. The Proposed multiplier topology](image)

In this topology the output current is computed as follows:
The output voltage is also computed as follows:

\[ V_{\text{out}} = I_{\text{out}} \times R = \left( (I_{D52} + I_{D56}) - (I_{D54} - I_{D58}) \right) R \]  

(3)

As a result, the output is as follows:

\[ I_{\text{out}} \approx 4 \left( \frac{(\eta-1)}{\eta V_{T}} \right)^{2} V_{i_{n2}} V_{i_{n1}} \]  

(4)

As shown through these mathematical equations, the proposed multiplier topology can perform four-quadrant multiplication. It should be noted that in each quadrant we have two differential input signals \( V_{i_{n1}} \) and \( V_{i_{n2}} \). For first one \( V_{i_{n1}} \) is \( V_{1} \) and \( V_{i_{n2}} \) is \( V_{2} \). In other three quadrants \( V_{i_{n1}} \) is \( V_{5}, V_{5} \) and \( V_{7} \), and \( V_{i_{n2}} \) is \( V_{4}, V_{6} \) and \( V_{8} \) respectively.

### 4 Simulation Results

To compare the performance of the proposed multiplier topology, we have used the 0.18 \( \mu \text{m} \) CMOS technology in threshold voltage of -0.443 V, two identical resistance 1MΩ, 0.15 V supply voltage, \( 10^{10} \) A \( I_{\text{BIAS}} \) (to bias the transistors in weak inversion) and the equal size transistors (W/L, 45 \( \mu \text{m} \) /2 \( \mu \text{m} \)). The bias voltage \( V_{b} \) in the proposed multiplier topology is 100mV.

The proposed topology is simulated using HSPICE simulator. Table 1 shows the simulation results of the proposed analog multiplier in comparison with [6, 9, 10].

<table>
<thead>
<tr>
<th>Parameters</th>
<th>This paper</th>
<th>[6]</th>
<th>[10]</th>
<th>[9]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18 [μm]</td>
<td>0.35 [μm]</td>
<td>0.18 [μm]</td>
<td>0.35 [μm]</td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>0.15 [V]</td>
<td>3.3 [V]</td>
<td>0.5 [V]</td>
<td>1.5 [V]</td>
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<tr>
<td>( V_{b} )</td>
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<td>400 [mV]</td>
<td>NA</td>
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<td>( I_{\text{BIAS}} )</td>
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<td>10 [μA]</td>
<td>300 [nA]</td>
<td>NA</td>
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<tr>
<td>Input range</td>
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<td>±[NA]</td>
<td>±80 [mV]</td>
<td>±120 [mV]</td>
</tr>
<tr>
<td>Power</td>
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<td>0.34 [mW]</td>
<td>714.3 [nW]</td>
<td>6.7 [μW]</td>
</tr>
</tbody>
</table>
Based on our simulation results which are shown in table 1, the proposed analog multiplier has power consumption advantage compared to other multipliers in [6, 9, 10].

5 Conclusions

A CMOS four quadrant analog multiplier is presented which works in weak inversion by driving it at bulk terminals. The proposed multiplier is suitable for low power applications. The simulation results show that the proposed analog multiplier provided significantly improvement on the power consumption in comparison with other analog multipliers [6, 9, 10].

References